Hongzheng Tian

hongzhet@uci.edu | clanktian@gmail.com | +1-951-202-2793
github.com/hongzhengTian | linkedin.com/in/hongzhengtian/ hongzhengtian.com/

Education

- **University of California, Irvine (UCI), CA, USA** Sep. 2022 - Jun. 2027 (expected)
  Program: Ph.D. in Computer Engineering
- **University of California, Irvine (UCI), CA, USA** Sep. 2020 - Jun. 2022
  Program: Master's Degree in Computer Engineering
- **University of California, Riverside (UCR), CA, USA** Aug. 2019 - Jun. 2020
  Program: UCR-Graduate Preparation Program in Engineering (UCR-GPP-E)
- **University of British Columbia (UBC), BC, Canada** Jul. 2018 - Aug. 2018
  Program: Vancouver Summer Program in Communication Systems and Digital Systems Design with FPGA
- **Northwestern Polytechnical University (NWPU), Shaanxi, China** Sep. 2016 - Jun. 2020
  Program: Bachelor of Engineering's Degree in Microelectronics Science and Engineering

Scholarships & Rewards

- **Best Paper Award - Artifact Track, ICPE'25** May. 2025
- **Nominated of Electrical Engineering and Computer Science Professor/Graduate Student/Undergraduate Student of the Year Award, UCI** Mar. 2024
- **Second-class Scholarship for Outstanding Student, NWPU** Dec. 2017 & Dec. 2018
- **Second Prize, The 19th Undergraduate Mathematical Contest in Modelling, NWPU** Jun. 2018

Skills

- **Languages:** C, C++, OpenMP, Python, Verilog HDL, VHDL and MATLAB
- **Softwares & Tools:** Xilinx Design Tools, Synopsys, Candence, Quartus, ModelSim, and MATLAB

Researches & Publications

- **HeteroBench: Multi-kernel Benchmarks for Heterogeneous Systems** Mar. 2024 - Aug. 2024

  Project jointly supervised by the CORSA Lab, UCI & Hewlett Packard Labs

  Advisor: Professor Sitao Huang & Dr. Alok Mishra

  Summary: Build a cross-platform benchmark suite for evaluating heterogeneous HPC workloads across CPUs, GPUs, and FPGAs using Python, OpenMP, CUDA, and HLS

  Publication: ICPE'25 & SPEC RG Tools

  Award: Best Paper Award - Artifact Track

- **CoVA: An MLIR-Based Compilation Flow for Versatile Architecture** Jun. 2023 - Sept. 2023

  Project jointly supervised by the CORSA Lab, UCI & Hewlett Packard Labs

  Advisor: Professor Sitao Huang & Dr. Alok Mishra

  Summary: Build a MLIR-based compiling flow for heterogeneous backend devices, enhancing code portability and efficiency

  Publication: SC'24 ACM Student Research Competition Poster

- **A Sparsity-Aware Autonomous Path Planning Accelerator with Algorithm-Architecture Co-Design** Jan. 2023 - Sep. 2023

  Project jointly supervised by the CORSA Lab, UCI & the School of Cyberspace Science and Technology, Beijing Institute of Technology, BIT

  Advisor: Professor Sitao Huang & Professor Yanjun Zhang & Dr. Bo Yu

  Summary: Implement the Attention module based on the Versal ACAP AI Engines, with kernel fusion method applied

  Publication: ICCAD'24, FPGA'24 Poster Accepted

- **PyAIE: a Python-based Programming Framework for Versal ACAP AI Engines** Sep. 2022 - Jun. 2023

  Project at the CORSA Lab, UCI

  Advisor: Professor Sitao Huang

  Summary: Building a Python-based code generator targeting Versal ACAP AI Engines

  Publication: DAC'23 Late Breaking Results

- **Design Exploration of Associative Processor Implementation on FPGA** Apr. 2021 - Feb. 2022

  Project at the Lab of Center for Embedded and Cyber-physical Systems, UCI

  Advisor: Professor Fadi J. Kurdahi & Dr. Mohammed E. Fouda & Dr. Minjun Seo

  Summary: Built a new FPGA implementation of associative processor

  Publication: ISCAS'23 (Conference paper accepted)& IEEE TCAS-II (Journal accepted)

Internships

- **CoVA: An MLIR-Based Compilation Flow for Versatile Architecture** Jun. 2023 - Sep. 2023

  Employer's name: Hewlett Packard Enterprise, **Job title:** Research Associate Intern

  Summary: Build an MLIR-based compiling flow for heterogeneous backend devices, enhancing code portability and efficiency

  Duties & Achievements:

  - Learned MLIR framework and compilation flow from MLIR to LLVM IR, including Python bindings integration
  - Designed custom MLIR dialects to abstract program semantics from hardware specifics, enabling integration of high-level languages (Python, C/C++, Fortran)
  - Implemented analysis and transformation passes for optimization and lowering to multiple heterogeneous backends, including CPUs, GPUs, and FPGAs
  - Built a flexible compilation flow to improve portability and performance across diverse hardware platforms

- **HeteroBench: A Benchmark Suite for Heterogeneous Computing Systems** Jun. 2024 - Sep. 2024

  Employer's name: Hewlett Packard Enterprise, **Job title:** Research Associate Intern

  Summary: Develop a benchmarking framework to evaluate performance and scalability across heterogeneous computing platforms

  Duties & Achievements:

  - Designed and implemented a benchmark suite for evaluating heterogeneous systems across CPUs, GPUs, and accelerators
  - Developed profiling and measurement methodologies to capture performance, scalability, and resource utilization across diverse workloads
  - Conducted various experimental evaluations to analyze system behavior of different scheduling/execution strategies
  - Provided insights into performance variability across architectures, supporting system optimization and scheduling research

- **Design of MQ Decoder for a Real-Time JPEG2000 Player Based on FPGA** Sep. 2021 - Jan 2022

  Employer's name: IMBED LCC, **Job title:** Development Engineer trainee

  Summary: Designed a real-time JPEG2000 player for digital cinema applications

  Duties & Achievements:

  - Implemented the C code of the JPEG2000 decoder according to the JPEG2000 official document
  - Wrote and simulated the tier-1 entropy decoder (MQ decoder) in Verilog HDL
  - Learned from the relevant literature about the current improvement methods for MQ decoders
  - Optimized the basic version decoder to meet the timing and throughput constraints
  - Valuated its performance, which is up to 450 MHz

Undergraduate Projects

- **Design of Digital Multi-Channel Lock-in Amplifier based on FPGA** Sep. 2019 - Mar. 2020

Senior design at the Bourns College of Engineering, UCR

Advisor: Professor Shane Cybart

Summary: Co-designed a multi-channel lock-in amplifier based on FPGA which extract the desired signal with a known carrier wave from an environment that contains extremely noisy

Duties & Achievements:

- Designed the digital phase-locked loop to synchronize the external input reference signal
- Designed the reference signal generator to generate the internal reference square signal
- Designed the vector calculator to deal with the output vectors from the IIR filter
- The final system can extract 0.5 uV tiny sinusoidal signal from 500 mVpp white noise

• Design of Convolutional Neural Network (CNN) based on FPGA Sep. 2019 - Dec. 2019

Research at the Bourns College of Engineering, UCR

Advisor: Professor Philip Brisk

Summary: Assisted in the design of an FPGA-based Convolutional Neural Network for processing medical images

Duties & Achievements:

- Self-studied artificial intelligence and CNN related knowledge and got familiar with the C++ code of the CNN that the lab has completed
- Learned how to improve the speed of CNN based on the FPGA
- Learned how to use Vivado HLS to translate the high-level language to Verilog HDL and packaged the design as an IP for further tests and experiments

• Design of a Q-Learning Algorithm to solve the Find-Path Problem May. 2020 - Jun. 2020

EE XRC260 Course project, UCR

Advisor: Professor Sheldon Tan

Summary: Built a program that can find the correct path of a maze by using the Q-Learning algorithm

Duties & Achievements:

- Studied the basic knowledge of Reinforcement Learning
- Learned the basic algorithm of the Markov decision process and the Deep Q-Learning
- Implemented the algorithm via MATLAB and designed a program to find the shortest and correct path out of the maze.

• Design and Manufacture of AF/MF Radios May. 2018 - Jun. 2018

Electronic practice at Training Center of Engineering, NWPU

Duties & Achievements:

- Explored the principles and structures of AM/FM radios
- Learned welding skills for electronic components
- Welded a radio and completed related commissioning and assembly work

• Undergraduate Mathematical Contest in Modelling, Northwestern Polytechnical University May. 2018

- Design a mathematical model by using cluster analysis and hierarchical analysis to analyze the text from the topology structure and logical structure
- Use MATLAB programming to count the frequency of each character in each paragraph to determine whether the contents of a book were written by the same author

Activities

• Young Fellow Program of the 60th Design Automation Conference Poster presentation

• SC24 ACM Student Research Competition Poster presentation

• LATTE'23, Workshop on Languages, Tools, and Techniques for Accelerator Design

Tian, Hongzheng, Shining Yang, Yoonha Cha, and Sitao Huang. "PyAIE: A Python-based Compiler Framework for Versal ACAP Platforms." PyAIE-Youtube

Related Courses

• At University of California, Irvine:

- EECS 222 Embedded System Modeling: A
- EECS 226 Embedded System Software: A
- EECS 221 Languages and Compilers for Hardware Accelerators: A

• At University of California, Riverside:

- EE XRC 139 Solid-state Electronics: A
- EE XRC 146 Computer Vision: A
- EE XRC 168 Introduction of VLSI Design: A+
- EE XRC 260 Seminar in Electrical Engineering (Advanced VLSI): A+

TAs

• EECS 112 Computer Architecture, Fall 2023.

Extracurricular Activities

• Theory Department Undersecretary & Photography Team Leader, Astronomical Society, NWPU Aug. 2017 - Jun. 2018

- Taught starry sky photography knowledge and organized teammates to conduct starry sky photography during field inspections and contribute their works to various platforms of the university
- Taught and popularized astronomical knowledge by organizing related lectures and competitions
- Selected topics for the Starry Sky Carnival Competition while assuming the posts of question setter and judge for the Astronomical Joint Competition for Universities and Colleges in Shaanxi Province

• Learning Department Secretary, Student Union of School of Software and Microelectronics, NWPU Aug. 2017 - Jun. 2018

- Organized school activities and affairs with department members
- Solved learning problems for students to clarify their doubts
- Hosted learning experience exchange meetings and academic lectures for a good academic atmosphere
- Organized subject knowledge competitions and debate contests by selecting and training debaters
- Set questions for one advanced mathematics exam, invigilated it, and marked the exam papers